REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 2, 4-10, 23, 25, and 28-37 are in this application. Claims 1, 3, 11-22, 24 and 26-27 have been cancelled. Claims 2, 4-5, 7-8, 10, 23, 25, and 28-30 have been amended. Claims 35-37 have been added to alternately and additionally claim the present invention. In addition to the amendments discussed below, the claims have been amended to further clarify and alternately claim the present invention. These amendments were not made for reasons of patentability.

The Examiner objected to the drawings under 37 CFR §1.83(a) because claim 3 recites an adhesive which is not shown in the drawings. As noted above, claim 3 has been cancelled.

The Examiner rejected claims 2, 4, 9-10, 19, and 29-30 under 35 U.S.C. §103(a) as being obvious over Farnworth (U.S. Patent Publication No. US 2003/0106209 A1) in view of Kishimoto (U.S. Patent Publication No. US 2001/0048980 A1). The Examiner also rejected claims 2, 6, and 19-20 under 35 U.S.C. §103(a) as being obvious over Lin (U.S. Patent Publication No. US 2002/0105076 A1) in view of Kishimoto.

The Examiner further rejected claims 4-5 and 7-8 under 35 U.S.C. §103(a) as being obvious over Lin in view of Kishimoto and further in view of Lu et al. (U.S. Patent No. 6,100,573). In addition, the Examiner rejected claims 23, 25, and 29-32 under 35 U.S.C. §103(a) as being obvious over Akram et al. (U.S. Patent No. 6,022,750) in view of Kishimoto (U.S. Patent Publication No. US 2001/0048980 A1).

The Examiner also rejected claims 31-34 under 35 U.S.C. §103(a) as being obvious over Akram et al. in view of Kishimoto and further in view of Akram II (U.S. Patent No. 5,419,807). (The Examiner additionally rejected claim 3 under 35 U.S.C. §103(a) as being obvious over Lin et al. in view of Kishimoto and further in view of Yin et al. (U.S. Patent Publication No. US 2003/0049882). As noted above, claim 3

has been cancelled.) For the reasons set forth below, applicant respectfully traverses these rejections.

Claim 2, which has been amended, recites:

> "a die having:
> "a semiconductor structure that includes a substrate and a plurality of device regions formed in the substrate, the device regions being conductive; and
> "an interconnect structure that contacts the semiconductor structure, and forms a top surface of the die, the interconnect structure including:
> "a dielectric structure;
> "a plurality of layers of metal that are formed in and isolated by the dielectric structure, each metal layer having a plurality of metal traces that are electrically connected to the device regions; and
> "a plurality of bond pads that touch the dielectric structure, the plurality of bond pads being electrically connected to a plurality of metal traces; and
> "a conductive region having a bottom surface adhered to only a non-conductive region of the top surface of the die above the plurality of layers of metal, the conductive region including silicon and being spaced apart from the plurality of bond pads."

With respect to Farnworth/Kishimoto, the Examiner pointed to the Kishimoto reference as teaching the conventional metal interconnect structure of a die, and the Farnworth reference as teaching a conductive region that is formed over a die. Specifically, the Examiner pointed to die 92 shown in, for example, FIG. 5 of Farnworth as constituting the die required by claim 2, and contact member 118A shown in FIG. 5 of Farnworth as constituting the conductive region required by claim 2. The Farnworth reference, however, fails to teach or suggest a conductive region with a bottom surface that is adhered to only a non-conductive region of the top surface of the die.

As shown in FIG. 5 of Farnworth, contact member 118A is connected to only electrically conductive bond pad 120. Thus, rather than teaching a conductive region (118A) with a bottom surface that is adhered to only a non-conductive region

as required by claim 2, the Farnworth reference teaches that the conductive region (118A) is connected to only a conductive region.

Therefore, since the Farnworth and Kishimoto references do not teach or suggest a conductive region with a bottom surface that is adhered to only a non-conductive region of the top surface of the die, claim 2 is patentable over Farnworth in view of Kishimoto. In addition, since claims 4 and 9-10 depend either directly or indirectly from claim 2, claims 4 and 9-10 are patentable over Farnworth in view of Kishimoto for the same reasons as claim 2. (As note above, claim 19 has been cancelled.)

With respect to Lin/Kishimoto, the Examiner pointed to the Kishimoto reference as teaching the conventional metal interconnect structure of a die, and the Lin reference as teaching a number of bond/contact pads that are formed on the top surface of a die. Specifically, the Examiner pointed to the bond/contact pads 17 and 14 shown in FIGS. 2 and 4 of Lin as constituting the conductive region required by claim 2.

In addition, pointing to paragraph 0069 of Farnworth, the Examiner argued that a semiconductor integrated circuit does not necessarily include bond/contact pads. Based on this, the Examiner appears to argue that the bond/contact pads 17 and 14 shown in FIGS. 2 and 4 of Lin can be read to be the conductive region required by claim 2.

Applicant notes, however, that a wafer is singulated to form a die. Prior to singulation, the final fabrication steps of the wafer include forming a passivation layer, followed by the formation of a pad mask. Once the pad mask has been formed, openings are etched in the passivation layer to expose the bonding pads. (See "Silicon Processing for the VLSI Era, Volume 2: Process Integration," Stanley Wolf, Lattice Press, 1990, p. 337 attached in Appendix A; and paragraph 0010 of the Lin reference.)

Thus, since the pad mask is formed on the passivation layer, and the passivation layer is etched to expose the bonding pads before the wafer is

singulated, the resulting dice must necessarily include bonding pads. In addition, applicant can find nothing in paragraph 0069 of Farnworth that teaches or suggests that a wafer is first singulated and then, after the dice have been formed, each die is further individually processed to add bonding pads, an overlying passivation layer, and an etch step that exposes the bonding pads.

Therefore, a semiconductor integrated circuit must necessarily include a number of bond/contact pads. To remove any question, applicant has amended claim 2 to recite that the interconnect structure includes a plurality of bond pads, and the conductive region is spaced apart from the bond pads. As a result, the bond/contact pads 17 and 14 shown in FIGS. 2 and 4 of Lin can not be read to be the conductive region required by claim 2.

Thus, since neither the Lin nor the Kishimoto reference teaches or suggests the required conductive region, claim 2 is patentable over the Lin reference in view of the Kishimoto reference. In addition, since claim 6 depends either directly or indirectly from claim 2, claim 6 is patentable over Lin in view of Kishimoto for the same reasons as claim 2. (As note above, claims 19-20 have been cancelled.)

With respect to claims 4-5 and 7-8, these claims, which depend either directly or indirectly from claim 2, were rejected, in part, over Lin in view of Kishimoto as applied above. As a result, claims 4-5 and 7-8 are patentable over Lin in view of Kishimoto and further in view of Lu et al. for the same reasons that claim 2 is patentable over Lin in view of Kishimoto.

With respect to claim 23, this claim recites:

> "a die having:
> "a semiconductor structure that includes a substrate and a plurality of conductive regions formed in the substrate; and
> "an interconnect structure having a top surface, and a bottom surface that contacts the semiconductor structure, the interconnect structure having:
> "a dielectric structure,

"a plurality of metal interconnects formed within the dielectric structure, the metal interconnects making electrical connections with the plurality of conductive regions, and

"a test structure including:

"a first conductive region having a first surface adhered to an exterior surface of the interconnect structure and an opposing second surface;

"an insulation region having a first surface and an opposing second surface, the first surface of the insulation region contacting the second surface of the first conductive region; and

"a second conductive region having a first surface and an opposing second surface, the first surface of the second conductive region contacting the second surface of the insulation region, the second conductive region being electrically isolated from the first conductive region."

With respect to Akram/Kishimoto, the Examiner pointed to the Kishimoto reference as teaching the conventional metal interconnect structure of a die, and the Akram reference as teaching a test structure that is formed over a die. Specifically, the Examiner pointed to die 12 shown in, for example, FIG. 4 of Akram as constituting the die required by claim 23, and interconnect 16 shown in, for example, FIG. 3 of Akram as constituting the test structure required by claim 23. The Akram reference, however, fails to teach or suggest the insulation region and the second conductive region required by claim 23.

As taught by Akram, "interconnect 16 includes a pattern of conductors 58 and raised contact members 60. The raised contact members 60 are formed in a pattern that corresponds to test pads 62 (FIG. 4) on the die 12." (See column 4, lines 41-44 of Akram.) As shown in FIG. 4 of Akram, contact member 60 includes conductive layer 68, which is formed on a substrate 64. From what can be determined, however, there is no structure which can be read to be the insulation region or the second conductive region required by claim 23.

Thus, since neither the Akram nor the Kishimoto reference teaches or suggests the required insulation and second conductive regions, claim 23 is patentable over the Akram reference in view of the Kishimoto reference. In

addition, since claim 25 depends either directly or indirectly from claim 23, claim 25 is patentable over Akram in view of Kishimoto for the same reasons as claim 23.

With respect to claim 29, this claim recites:

> "a die having:
> 'a semiconductor structure having a substrate and a plurality of device regions formed in the substrate, the device regions being conductive; and
> "an interconnect structure that contacts the semiconductor structure, the interconnect structure having:
> "a dielectric structure;
> "a plurality of metal interconnects formed within the dielectric structure, the metal interconnects making electrical connections with the plurality of device regions, and
> "a plurality of bond pads that touch the dielectric structure, the plurality of bond pads being electrically connected to a plurality of metal traces; and
> "a test device having a bottom surface adhered to only a non-conductive region of an exterior surface of the die, the test device including a region of silicon and being spaced apart from the plurality of bond pads."

With respect to Farnworth/Kishimoto, the Examiner pointed to the Kishimoto reference as teaching the conventional metal interconnect structure of a die, and the Farnworth reference as teaching a test device. Specifically, the Examiner pointed to die 92 shown in, for example, FIG. 5 of Farnworth as constituting the die required by claim 29, and substrate 119 shown in FIG. 5 of Farnworth as constituting the test device required by claim 29. The Farnworth and Kishimoto references, however, fail to teach or suggest a test device that is adhered to only a non-conductive region of the exterior surface of the die.

As shown in FIG. 5 of Farnworth, substrate 119 is connected to only conductive bond pad 120. Thus, rather than teaching a test device (119) with a bottom surface that is adhered to only a non-conductive region as required by claim 29, the Farnworth reference teaches that the test device (119) is connected to only a conductive region.

Therefore, since the Farnworth and Kishimoto references do not teach or suggest a test device with a bottom surface that is adhered to only a non-conductive region of an exterior surface of the die, claim 29 is patentable over Farnworth in view of Kishimoto. In addition, since claim 30 depends directly from claim 29, claim 30 is patentable over Farnworth in view of Kishimoto for the same reasons as claim 29.

With respect to Akram/Kishimoto, the Examiner pointed to the Kishimoto reference as teaching the conventional metal interconnect structure of a die, and the Akram reference as teaching a test device that is formed over a die. Specifically, the Examiner pointed to die 12 shown in, for example, FIG. 4 of Akram as constituting the die required by claim 29, and interconnect 16 shown in, for example, FIG. 3 of Akram as constituting the test device required by claim 29. The Akram reference, however, fails to teach or suggest a test device with a bottom surface that is adhered to only a non-conductive region of the exterior surface of the die.

As further noted above, FIG. 4 of Akram shows the raised contact members 60 of interconnect 16. (See column 4, lines 41-44 of Akram.) However, as shown in FIG. 4 of Akram, contact member 60 is connected to only conductive pad 62. Thus, rather than teaching a test device (16/60) with a bottom surface that is adhered to only a non-conductive region as required by claim 29, the Akram reference teaches that the test device 16/60 is connected to only a conductive region.

Therefore, since the Akram and Kishimoto references do not teach or suggest a test device with a bottom surface that is adhered to only a non-conductive region of the die, claim 29 is patentable over Akram in view of Kishimoto. In addition, since claims 30-32 depend either directly or indirectly from claim 29, claims 30-32 are patentable over Akram in view of Kishimoto for the same reasons as claim 29.

With respect to claims 31 and 33-34, these claims, which depend either directly or indirectly from claim 29, were rejected, in part, over Akram in view of Kishimoto as applied above. As a result, claims 31 and 33-34 are patentable over

Akram in view of Kishimoto and further in view of Akram II for the same reasons that claim 2 is patentable over Akram in view of Kishimoto.

The Examiner objected to claim 28, but indicated that claim 28 would be patentable if amended to be in independent format to include all of the limitations of the base claim and any intervening claims. Claim 28 has been amended to be in independent format, but does not include all of the limitations of the base and intervening claims. However, claim 28 is believed to be patentable due to the requirement for a third opening. Further, new claims 35-37 depend either directly or indirectly from claim 28 and are patentable for the same reasons as claim 28.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are requested.

Respectfully submitted,

Dated: 9-8-05 By: Mark C. Pickering

Mark C. Pickering
Registration No. 36,239
Attorney for Assignee

P.O. Box 300
Petaluma, CA 94953-0300
Telephone: (707) 762-5500
Facsimile: (707) 762-5504
Customer No. 33402

APPENDIX A

SILICON PROCESSING

FOR

THE VLSI ERA

VOLUME 2:

PROCESS INTEGRATION

STANLEY WOLF Ph.D.
Professor, Department of Electrical Engineering
California State University, Long Beach
Long Beach, California

LATTICE PRESS

Sunset Beach, California

DISCLAIMER

This publication is based on sources and information believed to be reliable, but the authors and Lattice Press disclaim any warranty or liability based on or relating to the contents of this publication.

Published by:

Lattice Press,
Post Office Box 340
Sunset Beach, California 90742, U.S.A.

Cover design by Roy Montibon, Visionary Art Resources, Inc., Santa Ana, CA.

Library of Congress Cataloging in Publication Data
Wolf, Stanley

Silicon Processing for the VLSI Era
Volume 1 : Process Integration

Includes Index
1. Integrated circuits-Very large scale integration. 2. Silicon. I. Title

86-081923

ISBN 0-961672-4-5

9 8 7 6 5

PRINTED IN THE UNITED STATES OF AMERICA

$N_2 + H_2$ (5%) ambient for about 30 minutes. As a result, this step may also be used as the annealing process for reducing the interface trap density in the gate oxide that was introduced by earlier processing steps (see Vol. 1, chap. 7).

5.4.1.8 Passivation Layer and Pad Mask. Finally, a *passivation* (or *overcoat*) layer, such as CVD PSG or plasma-enhanced CVD silicon nitride, is put down onto the wafer surface. This layer seals the device structures on the wafer from contaminants and moisture, and also serves as a scratch protection layer.

Openings are etched into this layer so that a set of special metallization patterns under the passivation layer is exposed. These metal patterns are normally located in the periphery of the circuit and are called *bonding pads* (Fig. 5-16). Bonding pads are typically about 100 x 100 μm in size and are separated by a space of 50 to 100 μm. Wires are connected (bonded) to the metal of the bonding pads and are then bonded to the chip package. In this way connections are established from the chip to the package leads.

The bonding-pad openings are created by patterning the passivation layer with *Mask #7*. If a PSG layer is used, the phosphorus (2-6 wt%) in the glass not only causes the PSG to act as a getter for Na but also prevents the glass film from cracking. Care must be taken to ensure that not more than 6% phosphorus is incorporated into the PSG, as this can cause corrosion of the underlying metal if moisture enters the circuit package (see Vol. 1, chap. 10). When silicon nitride is used, care must be taken to ensure that the deposited nitride film exhibits low stress (either tensile or compressive), so that it will not crack, since cracking would compromise the sealing capability of the film.

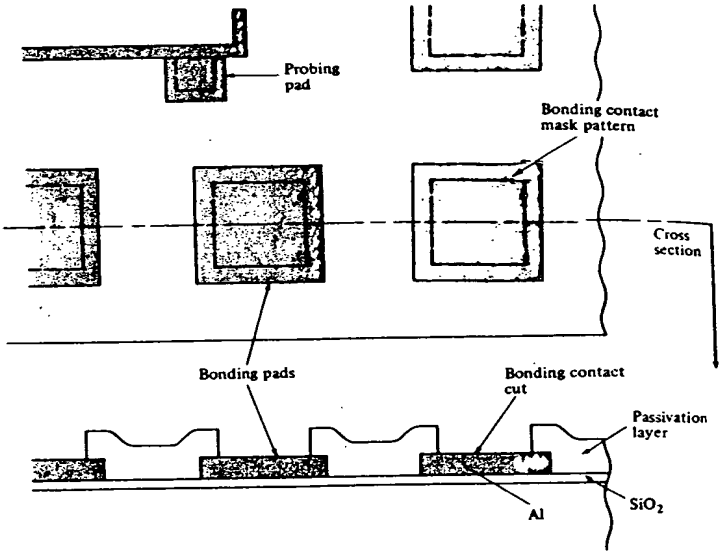

Fig. 5-16 Passivation layer and bonding pad openings. (Note, cross-section not to scale.)